EE/CprE/SE 492 WEEKLY REPORT 4

2/29/25 - 3/13/25

sdmay25-16

Project title: Multi-Channel High-Gain Low Noise Amplifier for High-Frequency Ultrasound Signal Acquisition

Client &/Advisor: Manojit Pramanik

Team Members/Role:

Jon Wetenkamp, Yash Gaonkar, Ethan Hulinsky, Ryan Ellerbach

- **Bi-Weekly Summary:**

Over the past two weeks, our team has been focused on finalizing both the PCB design and layout in EasyEDA. We dedicated significant time to refining the schematic, ensuring that all connections were correctly placed, and optimizing the board for manufacturability. Additionally, we worked on verifying component placements and routing to maintain signal integrity and minimize potential design issues.

During the most recent week, we met with our project contact to discuss key design aspects, address outstanding concerns, and provide an update on our progress. In this meeting, we reviewed the schematic in detail and clarified several critical points, including the required board thickness and the specific characteristics of the components we selected. With these details confirmed, we were able to move forward confidently with the board fabrication process.

After incorporating the final adjustments based on our discussion, we proceeded with ordering the PCBs. This marks a significant milestone in our project, as we transition from the design phase to physical implementation.

- **Past week accomplishments**
    - Yash Gaonkar: Researched electromagnetic (EM) shielding solutions to ensure compatibility with the new design. Currently finalizing the selection and integration of the Faraday cage to optimize shielding effectiveness.
    - Ethan Hulinsky: Updated layout to 4 layers and routed power to each amplifier. Compiled final BOM and generated Gerber files for PCB fabrication. Performed review of circuit and fixed some errors in the schematic, DRC and DFM checks before submitting order to ETG.
    - Ryan Ellerbach: Finished updating/creating footprints for the final components that will be used in the PCB design. Edited and fixed some final errors and polished things before purchasing our initial test board. Project management/organization.

- Jon Wetenkamp: Finished up work on the schematic. Might need minor changes in the future, but the first schematic should be done. Copied layout of channel 1 to remaining channels, created layout for single stage channels.

- **Pending issues**

  1) There are no pending issues at this time. We have successfully placed the order for the boards through ETG, and we are now awaiting their arrival. Once they are received, we will begin the assembly and testing process after spring break, ensuring that all components are properly integrated and the board functions as intended.

- **Individual contributions**

NAME	**Individual Contributions** *(Quick list of contributions. This should be short.)*	**Hours this week**	**HOURS cumulative**
Jonathan Wetenkamp	Made necessary changes to schematic, including bypass capacitors. Fixed minor issues in layout. Added via stitching to the entire layout to decrease noise. Added mounting holes. Ran DRC and corrected errors.	5.5	40
Yash Gaonkar	Researched EM shielding compatible with the new plan for board layout.	2	33.5
Ryan Ellerbach	Finished updating/creating footprints for the final components. Worked on editing and fixing some final errors. Project management and organization	4	41
Ethan Hulinsky	Updated layout to 4 layers and routed power to each amplifier. Compiled final BOM and generated Gerber files for PCB fabrication. Performed review of circuit and fixed some errors in the schematic, DRC and DFM checks before submitting order to ETG.	6	46

- **Plans for the upcoming week**

  Wait for the boards and components to come after spring break is over and start assembling the boards after spring break to test in the next few weeks. Plan for testing and power supply implementation.